What is claimed is:

1. A microprocessor equipped with a power control function, comprising:

a power control permission setting unit, which previously sets information as to whether or not a power control operation is carried out; and

a power control output controller, which finally controls an output of a power control signal in accordance with the information set in the power control permission setting unit when a power control instruction is executed, the power control instruction separately designating power control operations with respect to operation resources of the microprocessor.

2. The microprocessor as claimed in claim 1, further comprising:

a power control register, which stores information as to operation resources whose power control operations should be carried out, which are designated by the power control instruction;

a power control circuit, which outputs power control signals for controlling electric power with respect to the respective operation resources based on the information stored in the power control register; and

a gate circuit, which gates the respective power control signals in accordance with the information set to the power control permission setting unit.

3. A microprocessor equipped with a power control function, comprising:

a processor state judging unit, which holds information as to whether or not a power control operation is carried out, which has been previously set every program ID applied to each of instruction programs, and which judges as to whether or not a program ID of an instruction program under execution corresponds to the program ID which has been set so as to perform the power control operation; and

a power control output controller, which finally controls an output of a power control signal in accordance with a judgement result of the processor state judging unit as to the instruction program under execution when a power control instruction is executed, the power control instruction separately designating power control operations with respect to operation resources of the microprocessor.

4. The microprocessor as claimed in claim 3, further comprising:

a power control register, which stores information as to operation resources whose power control operations should be carried out, which are designated by the power control instruction;

a power control circuit, which outputs power control signals for controlling electric power with respect to the respective operation resources based upon the information stored in said power control register; and

a gate circuit, which gates the respective power control signals in accordance with the judgement result of the processor state judging unit.

5. An instruction converting apparatus for optimizing an instruction program so as to suitably execute the optimized instruction program by a predetermined microprocessor, comprising:

a power control manager, which extracts power control management information by referring to an instruction statement which is written in the instruction program;

a power control information analyzer, which detect an operation resource based upon the power control management information extracted by the power control manager, the operation resource being not actuated for an instruction section having a predetermined length when the predetermined microprocessor is operated; and

a power control instruction applier, which applies an instruction related to a power control operation to the instruction program based upon the detected result of the power control information analyzer.

6. The instruction converting apparatus as claimed in claim 5, wherein:

the power control management information contains information for designating said predetermined length of the instruction section; and the power control information analyzer

changes the predetermined length of the instruction section based upon the power control management information.

7. The instruction converting apparatus as claimed in claim 5, further comprising:

a instruction-independent operation resource table storing unit, which stores information as to whether or not each of the operation resources of the predetermined microprocessor is actuated every instruction;

wherein the power control information analyzer detects such an operation resource which is not actuated for the instruction section having the predetermined length when the predetermined microprocessor is operated based upon the information stored in the instruction-independent operation resource table storage unit.

8. A instruction converting apparatus for optimizing an instruction program so as to suitably execute the optimized instruction program by a predetermined microprocessor, comprising:

a power control analyzer, which detects an operation resource which is not actuated for an instruction section having a predetermined length when the predetermined microprocessor is operated; and

a power control instruction applier, which applies an instruction related to a power control operation to the instruction program based upon the detection result of the power

control information analyzer;

wherein the power control information analyzer comprises,

a instruction reassembling unit, which reassembles the instruction program in such a manner that an instruction section is made long, during which an actuation of an operation resource can be stopped.

9. The instruction converting apparatus as claimed in claim 8 wherein:

the instruction reassembling unit corresponds to instruction rearranging unit which rearranges instructions while maintaining an instruction dependent relationship established in the instruction program.

10. The instruction converting apparatus as claimed in claim 8 wherein:

the instruction reassembling unit corresponds to instruction replacing unit which replaces one instruction contained in the instruction program by a replaceable instruction having the same process result as that of the one instruction.

11. An instruction converting method for optimizing an instruction program so as to suitably execute the optimized instruction program by a predetermined microprocessor, comprising:

a power control managing step for extracting power control management information by referring to an instruction statement

which is written in the instruction program;

a power control information analyzing step for detecting an operation resource based upon the power control management information extracted in the power control managing step, the operation resource being not actuated for an instruction section having a predetermined length when the predetermined microprocessor is operated; and

a power control instruction applying step for applying an instruction related to a power control operation to the instruction program based upon the detected result of the power control information analyzing step.

12. The instruction converting method as claimed in claim 11 wherein:

the power control management information contains information for designating said predetermined length of the instruction section; and the power control information analyzing step changes the predetermined length of the instruction section based upon the power control management information.

13. The instruction converting method as claimed in claim 11, wherein:

the power control information analyzing step refers to an instruction-independent operation resource table which stores thereinto information as to whether or not each of the operation resources of the predetermined microprocessor is actuated every instruction in order to detect such an operation

resource which is not actuated for the instruction section having the predetermined length when said predetermined microprocessor is operated.

14. An instruction converting method for optimizing an instruction program so as to suitably execute the optimized instruction program by a predetermined microprocessor, comprising:

a power control analyzing step for detecting an operation resource which is not actuated for an instruction section having a predetermined length when said predetermined microprocessor is operated; and

a power control instruction applying step for applying an instruction related to a power control operation to the instruction program based upon the detection result of the power control information analyzing step; wherein:

the power control information analyzing step is comprised of: an instruction reassembling step for reassembling the instruction program in such a manner that an instruction section is made long, during which an actuation of an operation resource can be stopped.

15. The instruction converting apparatus as claimed in claim 14 wherein:

the instruction reassembling step rearranges instructions while maintaining an instruction dependent relationship established in the instruction program.

16. The instruction converting apparatus as claimed in claim 14 wherein:

the instruction reassembling step replaces one instruction contained in the instruction program by a replaceable instruction having the same process result as that of the one instruction.

17. A microprocessor wherein:

the microprocessor executes the instruction program converted by the instruction converting apparatus recited in any one of claim 5 to claim 10 so a to separately perform a power control operation with respect to an operation resource built in said microprocessor.

18. A microprocessor wherein:

the microprocessor executes the instruction program converted by the instruction converting method recited in any one of claim 11 to claim 16 so as to separately perform a power control operation with respect to an operation resource built in the microprocessor.